

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|----|------|-----|------|---|--|------------------|
| 6 | BRS | L6 | 5798 | (address same NV memory) and (cache same destination) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:25 |
| 7 | BRS | L7 | 4289 | (address same NV memory same cache same destination) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:26 |
| 8 | BRS | L8 | 0 | (address same NVmemory same cache same destination) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:26 |
| 9 | BRS | L9 | 1 | (address same NV same memory same cache same destination) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:26 |
| 10 | BRS | L10 | 401 | (NV adj memory) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:26 |

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|----|------|-----|------|--|--|------------------|
| 11 | BRS | L11 | 11 | (NV adj memory) same cache same controller | US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:27 |

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|--|--|------------------|
| 1 | BRS | L1 | 5 | 700/87.ccls. and NV | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:19 |
| 2 | BRS | L2 | 1 | 700/87.ccls. and (NV adj memories) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:19 |
| 3 | BRS | L3 | 22 | (NV adj memories) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:19 |
| 4 | BRS | L4 | 10 | (NV adj memories) and controller | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:20 |
| 5 | BRS | L5 | 9 | (NV adj memories) and controller and (read or writ\$5) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:20 |

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| 1 | BRS | L1 | 5 | 700/87.ccls. and NV | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:19 |
| 2 | BRS | L2 | 1 | 700/87.ccls. and (NV adj memories) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:19 |
| 3 | BRS | L3 | 22 | (NV adj memories) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB | 2007/02/06 14:19 |
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memory - group of 2 »

HG Sachs, JY Cho, WH Hollingsworth - US Patent 4,933,835, 1990 - Google Patents

... The data **cache**- MMU and instruction **cache**-MMU each have ... interfaces for coupling tothe main **memory** and to ... system bus, includ -ing an interrupt **controller**, an I ...[Cited by 93](#) - [Related Articles](#) - [Web Search](#)**Apparatus and method for performing error correction in a multi-processor system** - group of 2 »

NV Sarangdhar, KK Lai - US Patent 5,550,988, 1996 - Google Patents

... 210 DATA **CACHE** ... executed the programs stored in the main **memory** by fetchingtheirinstructions ... Forexample, in amulti-agentcomputer system, **word** processing ...[Cited by 26](#) - [Related Articles](#) - [Web Search](#)**Apparatus and method for caching lock conditions in a multi-processor system** - group of 3 »

... KK Lai, G Singh, MS Joshi, NV Sarangdhar, MA Fisch - US Patent 6,006,299, 1999 - Google Patents

... locations. In other **words**, an instruction may be fetched from **memory** locations spanning two **cache** lines. 50 However ...[Cited by 10](#) - [Related Articles](#) - [Web Search](#)**[PS] RAPID-cache-a reliable and inexpensive write cache for disk I/O systems** - group of 5 »

Y Hu, Q Yang, T Nightingale - Proceedings of the Fifth International Symposium on High- ... - eecs.uc.edu

... Using real-world traces as well as synthetic traces ... to assemble data from non-contiguous **memory** locations), then ... Reading is straightforward in RAPID-Cache. ...[Cited by 24](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

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NV memory cache word "controller"

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address NV memory cache destination word c

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Computer system and method for maintaining memory consistency in a pipelined, non-blocking caching ... - group of 3 »

... Brayton, MW Rhodehamel, NV Sarangdhar, GJ Hinton - US Patent 5,623,628, 1997 - Google Patents

... **memory** system. The **cache** consistency mechanism includes an external bus request queue which and associated mecha -nism, which cooperate to monitor and **control** ...

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... THAT ARE DISTRIBUTED AND/OR PROCESSED UNDER THE CONTROL OF A HOST MICROPROCESSOR BY A DIRECT MEMORY ... - group of 3 »

A Movshovich, RH Hoem, NA Puttaswamy, B Lai - US Patent 6,434,170, 2002 - Google Patents

... 73) Assignee: Koninklijke Philips Electronics NV, Eindhoven (NL ... comprise a contiguous

block of **memory** which are defined by a queue starting **address**, a queue ...

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DMA controller for memory scrubbing - group of 2 »

G Dearth, TD Bissett - US Patent 5,588,112, 1996 - Google Patents

... and the corrected data element is rewritten to the original storage **address**. ... preventing the accumu -lation of data element errors in the **memory**. ... IO _V _i Nv ...

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Stack oriented data processing device - group of 5 »

MC Vlot, PER Lippens - US Patent 6,502,183, 2002 - Google Patents

... 73) Assignee: Koninklijke Philips Electronics NV, Eindhoven (NL) ... nation register involved (eg an **address** register or ... 55 lions by a **memory address** or indirectly ...

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Base address generation in a multi-processing system having plural memories with a unified address ... - group of 3 »

KM Guttag, K Balmer, RJ Gove, CJ Read, JE Golston, ... - US Patent 5,761,726, 1998 - Google Patents

... processor and a memories whose unique addressable **memory** portion encompasses ... base

address registers, a set of index **address** registers and a ... INSTRUCTION **CACHE** ^ ...

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... access execution engine with indirect addressing of circular queues in addition to direct memory ... - group of 3 »

A Movshovich, RH Hoem, NA Puttaswamy, B Lai - US Patent 6,463,059, 2002 - Google Patents

... (73) Assignee: Koninklijke Philips Electronics NV, Eindhoven (NL ... performs the

demultiplexing operation by creating a set of direct **memory** access (DMA ... VCXO
CONTROL ...

Cited by 15 - Related Articles - Web Search

Video optimized media streamer with **cache** management - group of 2 »

WR Belknap, MR Henley, L Falcon Jr, TE Frayne, ML ... - US Patent 5,586,264, 1996 - Google Patents

... 36 TAPE AND FILE M6M T **MEMORY** 34 PC 16 ... STORAGE NODE CTRL. AND VIDEO FILE SYSTEM **CONTROL**

RAID BUFFER (VIDEO CACHE a DISK INTERFACE 45 DISK CTRL a RAID MAPPING ...

[Cited by 124](#) - [Related Articles](#) - [Web Search](#)

Linked cell discharge detector having improved response time - group of 2 »

MN Maan - US Patent 4,689,807, 1987 - Google Patents

... CON TR OL CO NV SP CONV LP ... U PDATE SOURC E ADDRESS ... These portions of the video signal

are not specified by the data stored within video memory 132, but rather ...

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Method and device for providing an instruction trace from an on-chip CPU using control signals from ... - group of 3 »

R Warren - US Patent 6,279,103, 2001 - Google Patents

... 20 Q LU ūLU 82- NI NV OS T 1 2 ^4 42 ... 256 -^ 1 240 -> 2C > ADDRESS REGISTER
242 ^ ->•

21 ... 26 90 -160 222 EXTERNAL MEMORY INTERFACE CONTROLLER FIG. 1 1 174 ...

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Data processing device having split-mode DMA channel - group of 2 »

MD Beck, LR Simar - US Patent 5,826,101, 1998 - Google Patents

... i 24 **CACHE** 32o 32d 34 RAM 16 1,2(... 3x —^ RAM 20 1 i 32o 32d f) s ... 20, 1998
Sheet 2 of

44 5,826,101 ADDRESS • ADDRESS FIG. ARBITRATION AND HANDSHAKING ...

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[J Mills](#)
[G Singh](#)

Computer system and method for maintaining memory consistency in a pipelined, non-blocking caching ... - group of 3 »

... Brayton, MW Rhodehamel, NV Sarangdhar, GJ Hinton - US Patent 5,623,628, 1997 - Google Patents

... **memory** system. The **cache** consistency mechanism includes an external bus request queue which and associated mechanism, which cooperate to monitor and **control** ...

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Storage controller having additional cache memory and a means for recovering from failure and ... - group of 3 »

BC Beardsley, SK Candelaria, BS Powers, MA Reid - US Patent 5,437,022, 1995 - Google Patents

... iMARK CAC UNAVAIL MARK NV SUSPER 1 ... an analogous function for direct access storage

devices nonvolatile **memory**. Storage **controller cache** performs ...

Cited by 40 - [Related Articles](#) - [Web Search](#)

Apparatus and method of handling race conditions in mesi-based multiprocessor system with private ... - group of 2 »

NV Sarangdhar, WH Wang, M Fisch - US Patent 5,551,005, 1996 - Google Patents

... cannot retire until the data is available from the **cache** or **memory** sub-system. ... In other **words**, **memory** references are not necessarily forwarded in the order ...

Cited by 38 - [Related Articles](#) - [Web Search](#)

IBM Memory Expansion Technology (MXT) - group of 11 »

RB Tremaine, PA Franaszek, JT Robinson, CO Schulz, ... - IBM Journal of Research and Development, 2001 - researchweb.watson.ibm.com

... this region after quieting the system and flushing the **cache** hierarchy to the main **memory**. ... a power outage that affects all hardware except the NV main **memory** ...

Cited by 39 - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

Write combining buffer for sequentially addressed partial line operations originating from a single ... - group of 2 »

MS Joshi, AF Glew, NV Sarangdhar - US Patent 5,630,075, 1997 - Google Patents

... program changes a value held in **memory**, it is performing ... **data cache controller** 203 and the **data cache** unit 204 ... In other **words**, instructions are not necessarily ...

Cited by 26 - [Related Articles](#) - [Web Search](#)

Apparatus for maintaining multilevel cache hierarchy coherency in a multiprocessor computer system - group of 3 »

... , G Singh, MW Rhodehamel, NV Sarangdhar, JM Bauer, ... - US Patent 5,715,428, 1998 - Google Patents

... requested and when the desired data **word** arrives ... K As will be seen, the present invention provides a **cache** ... **memory** hierarchy with complete support for **cache** coher ...

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Apparatus for maintaining consistency of a cache memory with a primary